CLAIM AMENDMENTS

1. (Currently Amended) A drive circuit for driving a power semiconductor device, said circuit comprising:

control means for controlling switching of the power semiconductor device according to a turn-on instruction or turn-off instruction sent to the power semiconductor device from outside said drive circuit;

~~controllable variable value detection means for detecting value of an electrical variable controlled by said control means and that is applied to a control terminal of the power semiconductor device during a time period when said control means receives a turn-on instruction;~~ and

abnormality detection means for ~~monitoring the~~ detecting value ~~detected by said controllable variable value detection means to detect~~ of at least one of a voltage that appears at a control terminal of the power semiconductor device and a current that flows into the control terminal of the power semiconductor device, and for detecting occurrence of an abnormality in the power semiconductor device when the value detected reaches an on-state value within a time period after receiving a turn-on instruction, the time period being shorter than a normal time period that elapses when the value detected reaches the on-state value after receiving a turn-on instruction in absence of an abnormality in the power semiconductor device.

Claims 2-4 (Cancelled).

5. (Currently Amended) The drive circuit according to Claim 1, wherein ~~, when~~ said abnormality detection means detects the voltage that appears at the control terminal of the power semiconductor device during a first time period from receiving the turn-on instruction and detects occurrence of an abnormality ~~, said control means causes~~ in the power semiconductor device ~~to make a transition to an off state~~ when the voltage detected reaches the on-state value within the first time period, the first time period excluding the normal time period during which, in the absence of an abnormality in the power semiconductor device, the voltage that appears at the control terminal of the power semiconductor device becomes equal to the on-state value.

6. (Currently Amended) The drive circuit according to Claim 5, wherein ~~, when~~ said abnormality detection means detects the current that flows into the control terminal of the power semiconductor device during a first time period from receiving the turn-on

instruction and detects occurrence of an abnormality~~, said control means causes~~ in the power semiconductor device~~ to make a transition to an off state at a lower speed than the speed at which said control means causes~~ when the current detected reaches the on-state value within the first time period, the first time period excluding the normal time period during which, in the absence of an abnormality in the power semiconductor device~~ to make a transition to an off state according to a turn-off instruction~~ the control current that flows into the control terminal of the power semiconductor device becomes equal to the on-state value.

7. (Currently Amended) A drive circuit for driving a power semiconductor device, said circuit comprising:

control means for controlling switching of the power semiconductor device according to a turn-on instruction or turn-off instruction sent to the power semiconductor device from outside said drive circuit;

~~controllable variable value detection means for detecting value of an electrical variable controlled by said control means and that is applied to a control terminal of the power semiconductor device;~~ and

abnormality detection means for~~ monitoring the~~ detecting value of~~ the electrical variable detected by said controllable variable value detection means to detect~~ at least one of a control voltage that appears at a control terminal of the power semiconductor device and a control current that flows into the control terminal of the power semiconductor device, and for detecting occurrence of an abnormality in the power semiconductor device~~, and for validating detection of the occurrence of an abnormality, only during a time period after said control means has received a turn-on instruction~~ when the value detected reaches an on-state value of the control voltage or the control current, wherein said abnormality detection means validates detection of the occurrence of an abnormality in the power semiconductor device only during a time period after receiving a turn-on instruction, the time period excluding a normal time period during which, in absence of an abnormality in the power semiconductor device, the control voltage that appears at the control terminal of the power semiconductor device or the control current that flows into the control terminal of the power semiconductor device becomes equal to the on-state value of the control voltage or the control current.

8. (New) The drive circuit according to Claim 1, wherein, when said abnormality detection means detects the occurrence of an abnormality in the power

semiconductor device, said control means causes the power semiconductor device to make a transition to an off state.

9. (New) The drive circuit according to Claim 1, wherein, when said abnormality detection means detects the occurrence of an abnormality in the power semiconductor device, said control means causes the power semiconductor device to make a transition to an off state at a lower speed than the speed at which said control means causes the power semiconductor device to make a transition to an off state according to a turn-off instruction.

10. (New) The drive circuit according to Claim 5, wherein the first time period excludes a recovery time period immediately following beginning of turning-on of the power semiconductor device.

11. (New) The drive circuit according to Claim 6, wherein the first time period excludes a recovery time period immediately following beginning of turning-on of the power semiconductor device.

12. (New) The drive circuit according to Claim 7, wherein the first time period excludes a recovery time period immediately following beginning of turning-on of the power semiconductor device.

13. (New) The drive circuit according to Claim 7, wherein, when said abnormality detection means detects the occurrence of an abnormality in the power semiconductor device, said control means causes the power semiconductor device to make a transition to an off state.

14. (New) The drive circuit according to Claim 7, wherein, when said abnormality detection means detects the occurrence of an abnormality in the power semiconductor device, said control means causes the power semiconductor device to make a transition to an off state at a lower speed than the speed at which said control means causes the power semiconductor device to make a transition to an off state according to a turn-off instruction.

15. (New) A drive circuit for driving a power semiconductor device, said circuit comprising:

control means for controlling switching of the power semiconductor device according to a turn-on instruction or turn-off instruction sent to the power semiconductor device from outside said drive circuit; and

abnormality detection means for detecting amount of charge supplied to a control terminal of the power semiconductor device during a time period after receiving the turn-on instruction, and for detecting occurrence of an abnormality in the power semiconductor device when, after lapse of the time period, the amount of charge detected is less than a reference value, the reference value being larger than a total amount of charge supplied to the control terminal of the power semiconductor device during turning-on of the power semiconductor device when an abnormality occurs in the power semiconductor device, wherein the time period is longer than a normal time period during which, in absence of an abnormality in the power semiconductor device, the total amount of charge supplied to the control terminal of the power semiconductor device reaches the reference value.

16. (New) The drive circuit according to Claim 15, wherein, when said abnormality detection means detects the occurrence of an abnormality in the power semiconductor device, said control means causes the power semiconductor device to make a transition to an off state.

17. (New) The drive circuit according to Claim 15, wherein, when said abnormality detection means detects the occurrence of an abnormality in the power semiconductor device, said control means causes the power semiconductor device to make a transition to an off state at a lower speed than the speed at which said control means causes the power semiconductor device to make a transition to an off state according to a turn-off instruction.